ROADMAP TO VLSI DESIGN

Get to know the emerging trends in and novel concepts of very large-scale integration (VLSI) design

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A system is nothing but an implementation of logic to regulate the output in response to the inputs. This helps in automation of various processes. The system can be electrical, mechanical, electronic, or a combination of any two or more types. Designing an ideal system is very difficult. An ideal system will:

1. Occupy less space
2. Operate at a high speed
3. Dissipate less power
4. Support modularity
5. Take very small time to market
6. Have a high cost-to-performance ratio
7. Be easily upgradable to new specifications

During the entire system design, many steps are involved. Design procedure of any system starts with the study of its feasibility, requirement analysis, and entire project planning (load distribution, time scheduling, etc) based on this information. This is followed by designing of the system architecture, detailing the system design, its implementation, testing, installation, and finally operation and maintenance.

What is VLSI?

VLSI means 'very large-scale integration.' It is an effort to integrate discrete component circuits in a single silicon base (chip). The integration results in a high reliability, low power consumption, less weight, low volume, and low cost of products.

The growing need for sophistication of applications continually pushes the design as well as manufacturing of electronic components and systems to a new level of complexity. For less complex operations, it is possible to design an electronic system using discrete components (transistors, gate ICs, etc). When we want very complex operations to be performed by the electronic system, it is very difficult to design the system using discrete components. The system becomes very bulky, unreliable, and less redundant. Also, it takes a lot of time to develop the system. Hence there is need to develop an integrated circuit or a single chip dedicated to a specific task. The chip is referred to as an application-specific integrated circuit (ASIC).

Xilinx Virtex-II XCV2800 industry's largest FPGA

A single chip has the following advantages over the circuit built from discrete components:

1. Size. Integrated circuits/chips are much smaller. Both transistors and wires are shrunk to micrometric (and nowadays to nanometric) sizes. Smaller components have smaller parasitic capacitances, resistances, and capacitances.

2. Speed. Communication within a chip can occur hundreds of time faster than communication between chips on a printed circuit board (PCB). This is because of smaller parasitic capacitances.

3. Power consumption. Due to smaller size, logic operation within a chip consumes less power.

These chip-level advantages result into a smaller physical size, low power consumption, and reduced cost of the system.

Introduction to ASIC

Before going deeper into an ASIC, let's first look at the evolution of silicon chip or intergraded circuit (IC). Fig. 1 shows an IC package. (This is a pin-grid array or PGA, shown upside down. The pins will go through holes in the PCB.) People often call this package a chip, but, as seen in Fig. 2, the silicon chip die itself is mounted in the cavity under the sealed lid. A PGA package is usually made from ceramic material, but plastic packages are more common.

TABLE I
Comparison Between CMOS and Bipolar Technologies

Factors	CMOS	Bipolar
Static power dissipation	Low	High
Input impedance	High	Low
Noise margin	High	Low
Packaging density	High	Low
Fan out	Low	High
Direction	Bidirectional device	Unidirectional device

The physical size of a silicon die varies from a few millimetres to over 2.5 cm (1 inch) on a side. However, we often measure the size of an IC by the number of logic gates (such as two-input NAND gates) or the number of transistors that the IC contains; for example, a 100k gate IC contains the equivalent of 100,000 two-input NAND gates.

The semiconductor industry has evolved from the first ICs of the early 1970s and matured rapidly since then. Early small-scale integration (SSI) ICs contained a few logic gates (1 to 100)—NAND gates, NOR gates, and so on—amounting to a few tens of transistors.

Medium-scale integration (MSI) increased the range of integrated logic (100 to 1000 logic gates on a single silicon chip) available to counters and similar large-scale logic functions.

Large-scale integration (LSI) ICs with 1000 to 10,000 logic gates on a single silicon chip packed even larger logic functions such as the first microprocessor into a single chip.

Very large-scale integration (VLSI) ICs with 10,000 to 100,000 logic gates on a single silicon chip offer 64-bit microprocessors, complete with cache memory and floating-point arithmetic units—well over a million transistors on a single piece of silicon. As CMOS process technology advances, transistors continue to get smaller and ICs hold more and more transistors.

The earliest ICs used bipolar technology and the majority of logic ICs used either transistor-transistor logic (TTL) or emitter-coupled logic (ECL). Initially it was difficult to manufacture metal-oxide-silicon (MOS) transistor because of problems with the oxide interface. As these problems were gradually solved, metal-gate n-channel MOS (NMOS or n MOS) technology developed in the 1970s. At that time, an MOS IC required fewer masking steps, was denser, and consumed lesser power than equivalent bipolar ICs. This means that for a given performance, an MOS IC cost lower than a bipolar IC, which led to growth of the MOS IC market.

TABLE II
Reduction in Feature Size Over the Years

Year	Feature size
1970	7 µm-10 µm
1970-80	5 µm
1980s	< 2 µm
1990s	< 1 µm (sub-micron process)

By the early 1980s the aluminium gates of transistors were replaced by polysilicon gates, but the name MOS remained. The introduction of polysilicon as a gate material was a major improvement in MOS technology, rendering it easier to make two types of transistors (n-channel MOS and p-channel MOS transistors) on the same IC. The technology was termed as complementary MOS (CMOS). One major advantage of a CMOS IC over NMOS IC is lower power consumption. Also, the polysilicon gate simplified the fabrication process, allowing devices to be scaled down in size. Comparison between CMOS and bipolar technologies is given in Table I.

A two-input NAND gate has four CMOS transistors. So to convert between gates and transistors, you multiply the number of gates by 4 to obtain the number of transistors. We can also measure an IC by the smallest feature size (roughly half the length of the smallest transistor) imprinted on the IC.

In manufacturing technology, the value of gate length (L) is called feature size. Gate length (refer Fig. 3) is measured in microns. (1 µm is one-millionth of a metre.) Thus when we say that an IC is built in (or with) a 0.5µm process, it means the gate length of a transistor is 0.5 µm. Table II shows the reduction in feature size over the years. Currently, feature size is 0.25 µm to 0.15 µm.

A modern sub-micron CMOS is now just as complicated as a sub-micron bipolar or BiCMOS (a combination of bipolar and CMOS) process. However, CMOS ICs are manufactured in much greater volume than any other technology and therefore, because of the economy of scale, the cost of a CMOS IC is less than of a bipolar or BiCMOS IC for the same function. Bipolar and BiCMOS ICs are still used for special needs. As these ICs are capable of han-

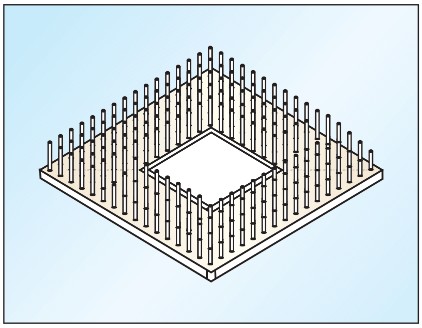


Fig. 1: An integrated circuit (IC)—a pin grid array (PGA) package

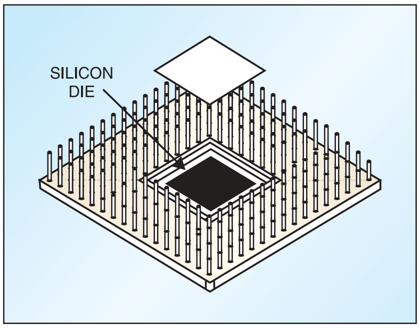
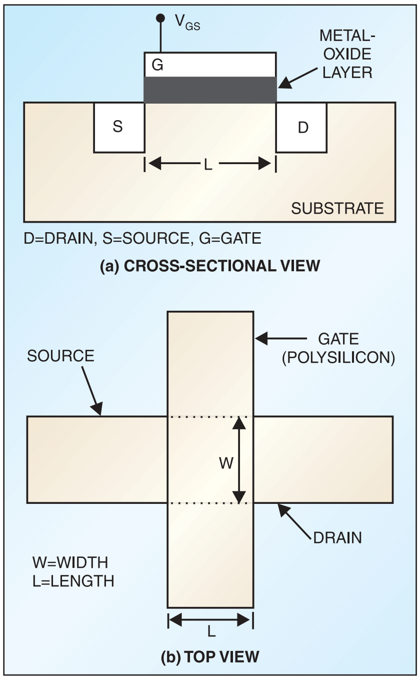


Fig. 2: The silicon die or chip is under the package lid



(a) CROSS-SECTIONAL VIEW

(b) TOP VIEW

Fig. 3: MOS transistor structure

dling higher voltages than CMOS, these are used in power electronics, cars, telephone circuits, and so on.

Some digital logic ICs and their analogue counterparts (analogue-to-digital converters) are standard parts or standard ICs. One can select standard ICs from the catalogues or from the data books and buy them from distributors. System manufacturers and designers can use the same standard part in a variety of different microelectronic systems (systems using ICs).

During 1980s engineers began to realise the advantages of designing an IC that was customised or tailored to a particular system or an application rather than using standard ICs alone. Thus the term 'microelectronic system design' came into picture. It is nothing but defining the functions that you can implement using standard ICs and then implementing the remaining logic functions with one or more custom ICs. Building a microelectronic system with fewer ICs allows you to reduce cost and improve reliability.

Of course, there are many situations in which it is not appropriate to use a custom IC for each and every part of a microelectronic system. For example, if you need a large amount of memory, it is still best to use standard memory ICs, either dynamic random-access memory (DRAM) or static RAM (SRAM), in conjunction with custom ICs. As different types of custom ICs began to evolve for different types of applications, these new ICs gave rise to application-specific ICs or ASICs.

Now IEEE international ASIC conference keeps track of the advances in ASICs. Since an ASIC is difficult to define, we shall look at some examples to help clarify what people in the IC industry understand by the term.

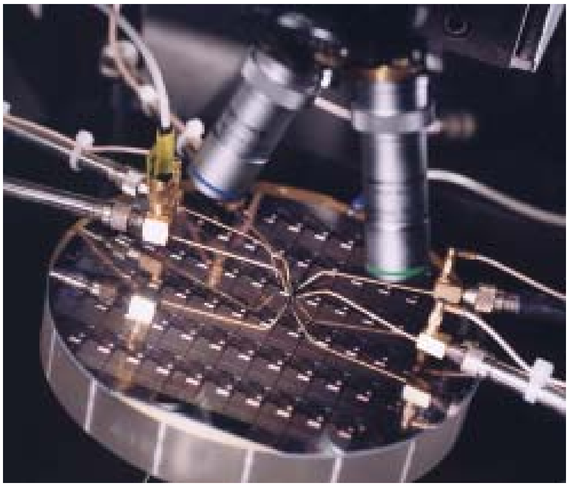
Standard ICs such as memory chips (ROMs, DRAMs, and SRAM), microprocessors, and TTL or TTL-equivalent ICs at SSI, MSI, and LSI levels are not called ASICs. Examples of ASICs include chips used in talking toy bears, satellites, cellular phones, and calculators, as well as chips handling the interface between the memory and the microprocessor in a workstation CPU, and chips containing a microprocessor and a cell together with other logic.

As a general rule, if you can find it in a data book, it is probably not an ASIC. But there are some exceptions. For example, two ICs that might or might not be considered as ASICs are the controller chip for PCs and the chip for modems. Both these ICs are specific to application but are sold to many different system vendors. ASICs are sometimes called as application-specific standard products.

Types of ASICs

ICs are made on a thin (a few hundred micron thick), circular silicon wafer, with the wafer holding hundreds of dies. The transistors and wirings are made from many layers (10 to 15 layers) built on top of one another. Each successive mask layer has a pattern defined using a mask similar to a glass photographic slide. The first half dozen or so layers define the transistors. The last half dozen or so layers define the metal wires between the transistors, i.e. the interconnects.

A full-custom IC includes some (sometimes all) logic cells that are customised and all mask layers that are customised. The microprocessor is an example of a full-custom IC. Full-custom ICs are the most expensive to manufacture and design. The manufacturing lead time, i.e. the time it takes just to make an IC (excluding the design time), is typically eight weeks for a full-custom IC. Full-custom ICs are often intended for a specific application, so designers might call some of them full-custom ASICs.


Advanced CMOS; courtesy: Philips

Designers are, however, more interested in semi-custom ASICs, in which all of the logic cells are predesigned and some (possibly all) of the mask layers are customised. Using predesigned cells from a cell library makes designers' task much easier. Semi-custom ASICs are classified into standard-cell based ASICs and gate-array based ASICs.

In programmable ASICs all of the logic cells are predesigned and none of the masked layers is customised. There are two types of programmable ASICs, namely, programmable logic devices (PLDs) and field-programmable gate arrays (FPGAs).

Full-custom ASICs. In a full-custom ASIC the engineer designs some or all of the logic cells, circuits, or layout specifically for one ASIC. This means the designer abandons the approach of using pretested and precharacterised cells for all or part of the design. It makes sense to take this approach only if there are no suitable cell libraries available that can be used for the entire design. This might be because existing cell libraries are not fast enough, or the logic cells are not small enough or consume a large power.

You may need to use full-custom design if the ASIC technology is new or so specialised that some circuits may be custom designed. Fewer and fewer full-custom ICs are being designed because of the problems with these special parts of the ASIC.

Standard cell-based ASICs. A cell-based ASIC (CBIC) uses predesigned logic cells (AND gates, OR gates, multiplexers, and flip-flops) known as standard cells. The standard cells in a CBIC fit together like bricks in a wall. The standard-cell areas may be used in combination with larger predesigned cells, such as microcontrollers or even microprocessors, known as mega cells. Mega cells are also called mega functions, full-custom blocks, system-level macros, fixed blocks, cores, or functional standard blocks.

ASIC designers define only the placement of standard cells and interconnects in CBICs. However, the standards cells can be placed anywhere on the silicon. This means that all the mask layers of the CBIC are customised and are unique to a particular customer.

With CBICs designers can save their time and money, and reduce risk by using predesigned, pretested, and precharacterised standard cells from library. In addition, each standard cell can be optimised individually. During the design of the cell library, each and every transistor can be chosen to maximise speed or minimise area. Manufacturing lead-time is about eight weeks.

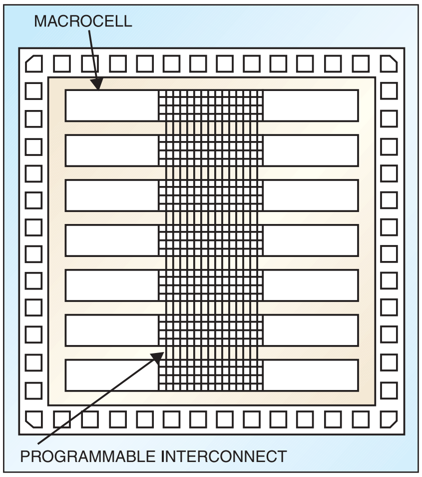


Fig. 4: A programmable logic device (PLD) die

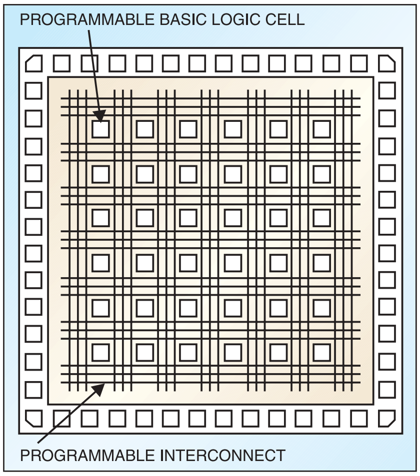


Fig. 5: A field-programmable gate array (FPGA) die

The disadvantages are the time or money spent on designing or buying the standard cell library, and the time consumed in fabricating all the layers of the ASIC for each new design.

Gate-array based ASICs. In gate-array based ASICs the transistors are predefined on the silicon wafer. The predefined pattern of transistors on a gate array is the base array, and the smallest element that is replicated to make the base array is the base cell. Only the top few layers of metal, which define the interconnects between the transistors, are defined by designers using custom masks. To distinguish this type of gate array from other types of gate arrays, it is often called the masked gate array (MGA).

MGA ASICs are classified into the following types:

1. Channelled gate arrays
2. Channelless gate arrays
3. Structured gate arrays

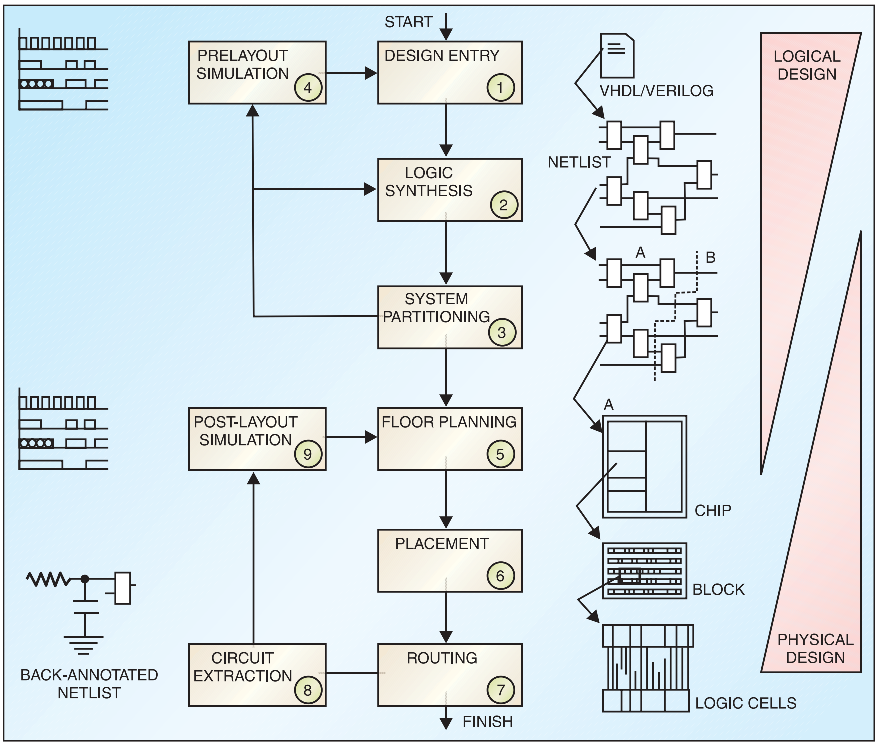


Fig. 6: An ASIC design flow

PLDs. PLDs are standard ICs that are available in standard configuration from a catalogue of parts and are sold in large volumes to many different customers. However, PLDs may be configured or programmed to create a part customised to a specific application, and so these also belong to the family of ASICs.

PLDs use different technologies to allow programming of the device. The most important features that all PLDs have in common are:

1. No customised masked layers or logic cells
2. Fast design turnaround
3. Single large block of programmable interconnects
4. A matrix of logic macrocells that usually consist of programmable array logic followed by a flip-flop or latch

A PLD die is shown in Fig. 4.

The simplest type of programmable IC is read-only memory (ROM). The programmable technologies used to make ROMs can be applied to more flexible logic structures. Using programmable devices in large arrays of AND gates and OR gates leads to creation of flexible and programmable logic devices called logic arrays.

Monolithic Memories was the first company to produce programmable array logic (PAL) devices for use, for example, as transition decoders for state machines. Since a PAL can also include registers (flip-flops) to store the current state information, you can use it to make a complete state machine.

Just as in masked programmable ROMs, designers placed a logic array as a cell on a custom ASIC. This type of logic array is called programmable logic array (PLA).

There is a difference between PLA and PAL: A PLA has a programmable AND logic array (AND plane) followed by a programmable OR logic array (OR plane). A PAL has a programmable AND plane and, in contrast to a PLA, a fixed OR plane.

FPGAs. FPGAs and PLDs are similar, except that the FPGA is usually larger and more complex than the PLD. In fact, some companies that manufacture programmable ASICs call their products FPGAs, while some call them complex PLDs (CPLDs).

FPGAs are the newest members of the ASIC family and are rapidly replacing TTL in microelectronic systems. Even though the FPGA is a type of gate array, the term gate-array based ASICs doesn't include FPGAs. This may change as FPGAs and MGAs start looking alike.

The essential characteristics of an FPGA are:

1. None of the mask layers is customised
2. A method for programming the basic logic cells and the interconnects
3. The core is a regular array of pro-

grammable basic logic cells that can implement combinational logic as well as sequential logic (flip-flops)

4. The matrix of programmable interconnects surrounds the basic logic cells

5. Programmable I/O cells surround the core

6. Design turnaround is a few hours

An FPGA die is shown in Fig. 5.

ASIC design flow

Fig. 6 shows the steps to design an ASIC. The steps are listed below with brief description:

1. Design entry. Enter the design into an ASIC design system, either by using hardware description language (HDL) or schematic entry.

2. Logic synthesis. Use an HDL (VHDL or Verilog) and a logic synthesis tool to produce a netlist; netlist is a description of logic cells and their connections.

3. System partitioning. Divide the large system into ASIC-size pieces.

4. Prelayout stimulation. Using stimulation tools such as Model Sim check whether the designed system functions correctly.

5. Floor planning. Arrange the blocks of netlist on the chip.

6. Placement. Decide the location of cells in a block.

7. Routing. Make the connections between cells and blocks.

8. Extraction. Determine the resistance and capacitance of the interconnections.

9. Post-layout stimulation. Check whether the design works with the added loads.

Steps 1 through 4 are part of logical design, and steps 5 through 9 are part of physical design. But there is some overlap; for example, system partitioning might be considered as either logical or physical design. In other words, when performing system partitioning, designers have to consider both logical and physical factors.

Conclusion

VLSI is an IC manufacturing technology, and VHDL and Verilog are the hardware description languages (programming languages) used to describe digital circuits. One has to write codes in VHDL or Verilog for a circuit and then download the same into CPLDs or FPGAs with the help of JTAG cable.

PLDs can be easily programmed, using development software running on a PC or workstation, to implement complex functions in digital systems. Because of programmability, PLDs shorten design development time. Engineers can design and program high-density PLDs in a matter of hours. PLDs also provide greater flexibility, allowing designers to adapt to changes in their design throughout the design process. This allows designers to fix design bugs in entry stages of production, and even add new features to the product while it is deployed in the field.

System-on-a-programmable chip solutions integrate PLDs and development tools, bringing about an efficient design flow. Some of the companies manufacturing CPLDs and FPGAs, and providing complete software tools for designing electronic systems are Xilinx, Altera, Lattice, Philips, and Analog Devices. ❑

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